METHOD AND SYSTEM FOR PIPELINE REDUCTION

Abstract of Disclosure

A method and system for operating a high frequency outprocessor with increased pipeline length. A new scheme is disclosed to reduce the pipeline by the detection and exploitation of so called "no_dependency" for an instruction. A "no dependency" signal tells that all required source data is available for the instruction at least one cycle before the source data valid bit(s) are inserted into the issue queue. Therefore, one or more stages of the pipeline are bypassed. Bypassing the pipeline stages for this "no dependency" conditions is especially important since a no dependency is found when the queue is empty. Furthermore, this bypass is very effective when the queue is relatively empty. Therefore, introducing such a bypass reduces effectively the performance drawback of a longer pipeline.

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